CLAIMS

What is claimed is:

1. A method to design a circuit, the method comprising:
determining first statistical circuit activity data at a plurality of nodes of a first design of the circuit;
transforming a first portion of the first design to generate a second portion of a second design of the circuit;
selectively determining at least one node in the second portion of the second design; and
determining second statistical circuit activity data for the at least one node in the second portion of the second design from the first statistical circuit activity data.

2. A method as in claim 1, wherein the first portion of the first design includes at least one of the plurality of the nodes of the first design.

3. A method as in claim 1, wherein the second statistical circuit activity data comprises:
a) probability information of state transition at a node;
b) probability information of the node being at a state; and
c) probability information of a group of nodes being at a state.

4. A method as in claim 1, wherein a subset of nodes of the plurality of nodes of the first design remain unchanged in the second design after the first portion of the first design is transformed; and, a portion of the first statistical circuit activity data is maintained for the subset of nodes in the second design.

5. A method as in claim 4, further comprising:

transforming a third portion of the second design to generate a fourth portion of a third design of the circuit;

selectively determining at least one node in the fourth portion of the third design; and

determining third statistical circuit activity data for the at least one node in the fourth portion of the third design from a portion of:

a) the first statistical circuit activity data; and

b) the second statistical circuit activity data.

6. A method as in claim 5, wherein one or more signals at the at least one node in the second portion of the second design drive the third portion of the second design.

7. A method as in claim 1, wherein the second statistical circuit activity data is determined from a formal Boolean analysis.

8. A method as in claim 1, wherein the first design is one of: a) a register transfer level (RTL) design, and b) a behavioral level design; and, the first portion of the first design is transformed to generate a gate level design.

9. A method as in claim 1, further comprising:
selectively determining the plurality of nodes of the first design.

10. A method as in claim 9, wherein the first statistical circuit activity data is obtained from a statistical analysis based on the first design.

11. A method as in claim 10, wherein the statistical analysis comprises one of:
a) a simulation based on a set of test vectors;
b) a simulation based on random input;
c) a formal analysis based on a specification of statistical input data.

12. A method as in claim 9, wherein the plurality of nodes comprise at least one of:
a) a register;
b) a finite state machine;
c) a counter;
d) a random access memory (RAM);
e) a set of registers with state constraints; and

f) a persistent node.

13. A method as in claim 9, further comprising:
determining state correlation information among the plurality of nodes of the first design;
wherein the second statistical circuit activity data is further determined from the state correlation information.

14. A method as in claim 1, wherein said transforming comprises one of:
a) replicating a register;
b) pushing a register through a logic element;
c) changing encoding of a finite state machine;
d) retiming; and
e) changing encoding of a group of nodes.

15. A method as in claim 14, wherein at least one node in the second portion of the second design comprises a register of the second portion of the second design.

16. A method as in claim 1, further comprising:
determining state correlation information among the at least one node in the second portion of the second design and a subset of nodes of the

plurality of nodes of the first design that remain unchanged in the second design after the first portion of the first design is transformed.

17. A machine readable medium containing executable computer program instructions which when executed by a digital processing system cause said system to perform a method to design a circuit, the method comprising:

determining first statistical circuit activity data at a plurality of nodes of a first design of the circuit;

transforming a first portion of the first design to generate a second portion of a second design of the circuit;

selectively determining at least one node in the second portion of the second design; and

determining second statistical circuit activity data for the at least one node in the second portion of the second design from the first statistical circuit activity data.

18. A medium as in claim 17, wherein the first portion of the first design includes at least one of the plurality of the nodes of the first design.

19. A medium as in claim 17, wherein the second statistical circuit activity data comprises:

a) probability information of state transition at a node;

b) probability information of the node being at a state; and

c) probability information of a group of nodes being at a state.

20. A medium as in claim 17, wherein a subset of nodes of the plurality of nodes of the first design remain unchanged in the second design after the first portion of the first design is transformed; and, a portion of the first statistical circuit activity data is maintained for the subset of nodes in the second design.

21. A medium as in claim 20, wherein the method further comprises:
transforming a third portion of the second design to generate a fourth portion of a third design of the circuit;
selectively determining at least one node in the fourth portion of the third design; and
determining third statistical circuit activity data for the at least one node in the fourth portion of the third design from a portion of:
a) the first statistical circuit activity data; and
b) the second statistical circuit activity data.

22. A medium as in claim 21, wherein one or more signals at the at least one node in the second portion of the second design drive the third portion of the second design.

23. A medium as in claim 17, wherein the second statistical circuit activity data is determined from a formal Boolean analysis.

24. A medium as in claim 17, wherein the first design is one of: a) a register transfer level (RTL) design, and b) a behavioral level design; and, the first portion of the first design is transformed to generate a gate level design.

25. A medium as in claim 17, wherein the method further comprises:
selectively determining the plurality of nodes of the first design.

26. A medium as in claim 25, wherein the first statistical circuit activity data is obtained from a statistical analysis based on the first design.

27. A medium as in claim 26, wherein the statistical analysis comprises one of:
a) a simulation based on a set of test vectors;
b) a simulation based on random input;
c) a formal analysis based on a specification of statistical input data.

28. A medium as in claim 25, wherein the plurality of nodes comprise at least one of:
a) a register;
b) a finite state machine;

c) a counter;

d) a random access memory (RAM);

e) a set of registers with state constraints; and

f) a persistent node.

29. A medium as in claim 25, wherein the method further comprises:

determining state correlation information among the plurality of nodes of the first design;

wherein the second statistical circuit activity data is further determined from the state correlation information.

30. A medium as in claim 17, wherein said transforming comprises one of:

a) replicating a register;

b) pushing a register through a logic element;

c) changing encoding of a finite state machine;

d) retiming; and

e) changing encoding of a group of nodes.

31. A medium as in claim 30, wherein at least one node in the second portion of the second design comprises a register of the second portion of the second design.

32. A medium as in claim 17, wherein the method further comprises:

determining state correlation information among the at least one node in the second portion of the second design and a subset of nodes of the plurality of nodes of the first design that remain unchanged in the second design after the first portion of the first design is transformed.

33. A data processing system to design a circuit, the data processing system comprising:

means for determining first statistical circuit activity data at a plurality of nodes of a first design of the circuit;

means for transforming a first portion of the first design to generate a second portion of a second design of the circuit;

means for selectively determining at least one node in the second portion of the second design; and

means for determining second statistical circuit activity data for the at least one node in the second portion of the second design from the first statistical circuit activity data.

34. A data processing system as in claim 33, wherein the first portion of the first design includes at least one of the plurality of the nodes of the first design.

35. A data processing system as in claim 33, wherein the second statistical circuit activity data comprises:

a) probability information of state transition at a node;

b) probability information of the node being at a state; and

c) probability information of a group of nodes being at a state.

36. A data processing system as in claim 33, wherein a subset of nodes of the plurality of nodes of the first design remain unchanged in the second design after the first portion of the first design is transformed; and, a portion of the first statistical circuit activity data is maintained for the subset of nodes in the second design.

37. A data processing system as in claim 36, further comprising:

means for transforming a third portion of the second design to generate a fourth portion of a third design of the circuit;

means for selectively determining at least one node in the fourth portion of the third design; and

means for determining third statistical circuit activity data for the at least one node in the fourth portion of the third design from a portion of:

a) the first statistical circuit activity data; and

b) the second statistical circuit activity data.

38. A data processing system as in claim 37, wherein one or more signals at the at least one node in the second portion of the second design drive the third portion of the second design.

39. A data processing system as in claim 33, wherein the second statistical circuit activity data is determined from a formal Boolean analysis.

40. A data processing system as in claim 33, wherein the first design is one of: a) a register transfer level (RTL) design, and b) a behavioral level design; and, the first portion of the first design is transformed to generate a gate level design.

41. A data processing system as in claim 33, further comprising:
means for selectively determining the plurality of nodes of the first design.

42. A data processing system as in claim 41, wherein the first statistical circuit activity data is obtained from a statistical analysis based on the first design.

43. A data processing system as in claim 42, wherein the statistical analysis comprises one of:
a) a simulation based on a set of test vectors;
b) a simulation based on random input;
c) a formal analysis based on a specification of statistical input data.

44. A data processing system as in claim 41, wherein the plurality of nodes comprise at least one of:

a) a register;

b) a finite state machine;

c) a counter;

d) a random access memory (RAM);

e) a set of registers with state constraints; and

f) a persistent node.

45. A data processing system as in claim 41, further comprising:

means for determining state correlation information among the plurality of nodes of the first design;

wherein the second statistical circuit activity data is further determined from the state correlation information.

46. A data processing system as in claim 33, wherein said means for transforming comprises one of:

a) means for replicating a register;

b) means for pushing a register through a logic element;

c) means for changing encoding of a finite state machine;

d) means for retiming; and

e) means for changing encoding of a group of nodes.

47. A data processing system as in claim 46, wherein at least one node in the second portion of the second design comprises a register of the second portion of the second design.

48. A data processing system as in claim 33, further comprising:

means for determining state correlation information among the at least one node in the second portion of the second design and a subset of nodes of the plurality of nodes of the first design that remain unchanged in the second design after the first portion of the first design is transformed.